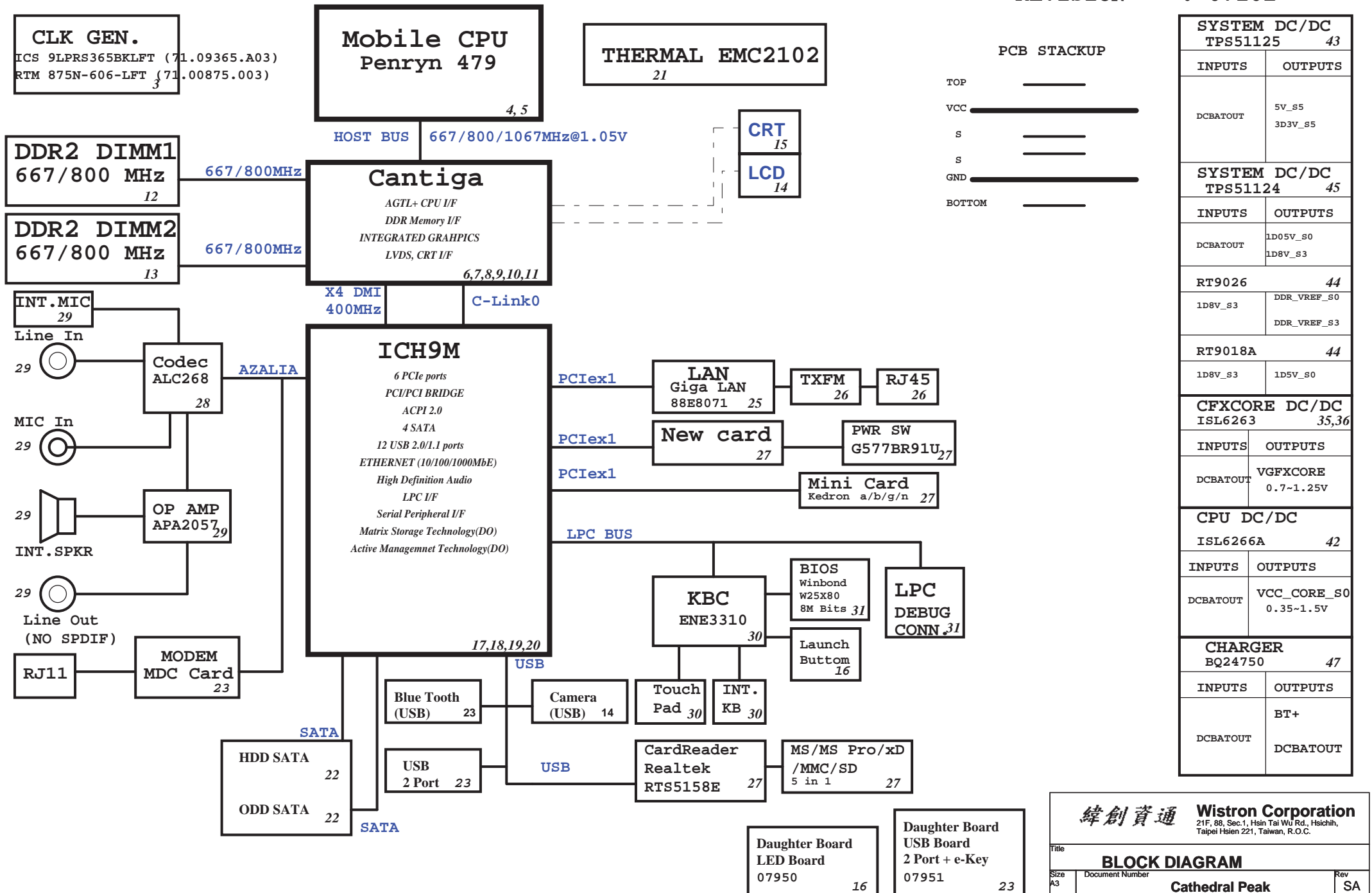


Cathedral Peak Block Diagram

Project code: 91.4J501.001
PCB P/N : 48.4J501.001
REVISION : 07261



<http://hobi-elektronika.net>

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BLOCK DIAGRAM			
Title	Document Number	Rev	SA
Size A3	Cathedral Peak		SA
Date: Monday, December 31, 2007	Sheet 1	of 41	

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#:SPI_CS1#/GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage. Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resistor.

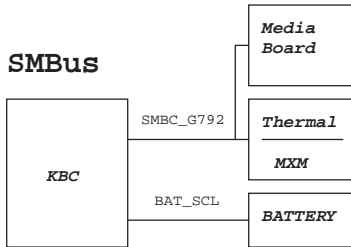
PCIE Routing

LANE1	LAN MARVELL 88E8071
LANE2	MiniCard WLAN
LANE3	NC
LANE4	NC
LANE5	NewCard
LANE6	NC

USB Table

USB	
Pair	Device
0	USB1
1	USB4
2	USB2
3	NC
4	USB3
5	Bluetooth
6	NC
7	MINIC1
8	WEBCAM
9	NEW1
10	Card Reader
11	NC

SMBus



ICH9M

SMBC_ICH

9LPRS365BKLEFT

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRS1PVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0 = The iTPM Host Interface is enabled(Note2) 1 = The iTPM Host Interface is disabled(default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. 1 = Normal operation(Default):Lane Numbered in order
CFG10	PCIE Loopback enable	0 = Enable (Note 3) 1 = Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation(Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3 DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display Port or PCIE is operational (Default) 1 = Digital display Port and PCIE are operating simultaneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 =No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1 = LFP Card Present; PCIE disabled

NOTE:

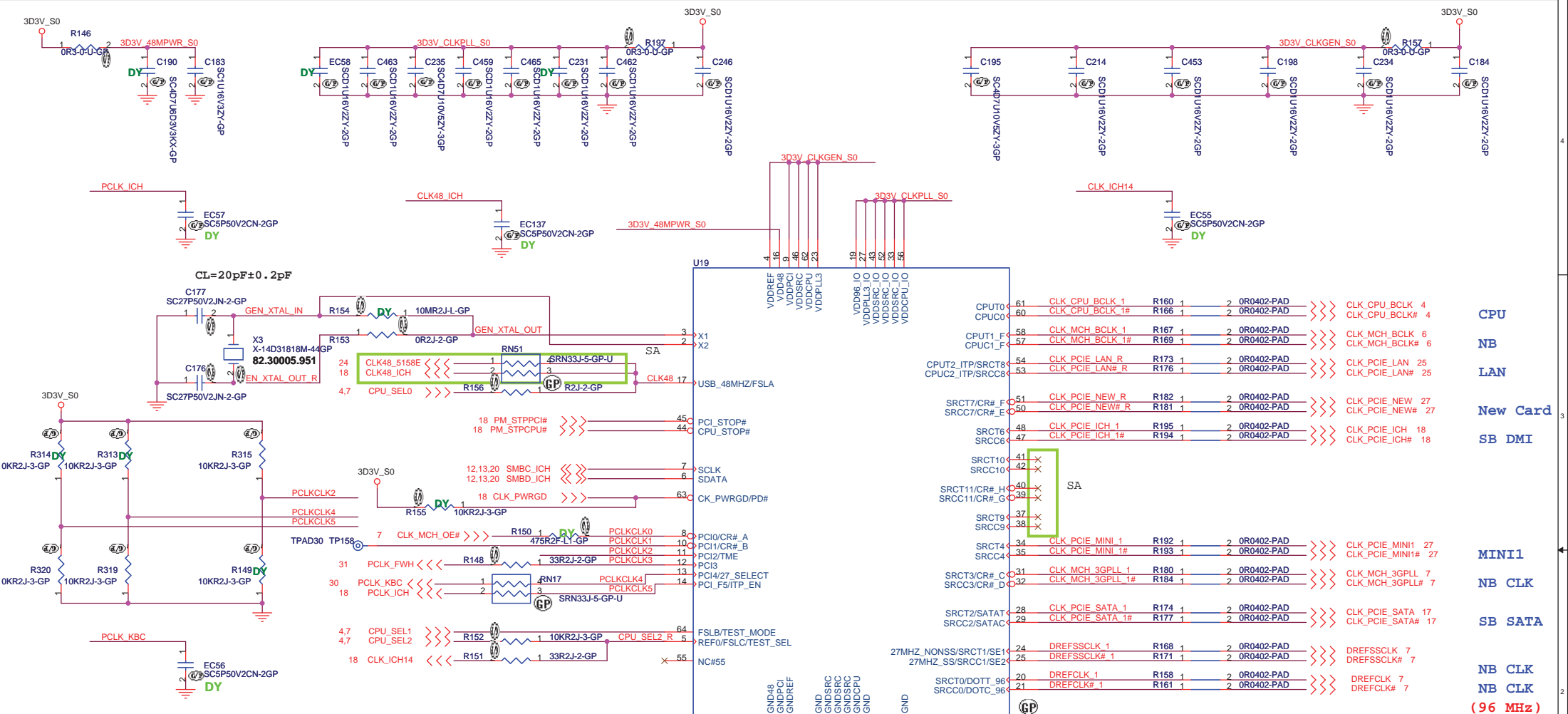
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

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Reference			
Title	Document Number	Rev	
Size A3	Cathedral Peak	SB	
Date: Monday, November 26, 2007	Sheet 2 of 41		

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ICS9LPRS365BKLFT setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1 = CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1 = CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1 = CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1 = CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	3.3V PCI clock output
PCI4/27M_SEL	0 = Pin24 as SRC-1, Pin25 as SRC-1#, Pin20 as DOT96, Pin21 as DOT96# 1 = Pin24 as 27MHz, Pin25 as 27MHz_SS, Pin20 as SRC-0, Pin21 as SRC-0#
PCI_F5/ITP_EN	0 = SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1 = CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1 = CR#_C controls SRC2 pair

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1 = CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1 = CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7# enabled (default) 1 = CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1 = CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1 = CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1 = CR#_H controls SRC10

SEL2	SEL1	SEL0	CPU	FSB
FSC	FSB	FSA		
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1066M

緯創資通 Wistron Corporation

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Title

Clock Generator

Size

Document Number

Cathedral Peak

Rev

SA

Date: Friday, January 11, 2008

Sheet 3 of 41

6 H_A#(35..3) <<< H_A#(35..3)

6 H_ADSTB#0 <<< H_REQ#(4..0) <<<

6 H_ADSTB#1 <<< H_A20M# <<< H_FERR# <<< H_IGNNE# <<< H_STPCLK# <<< H_INTR# <<< H_NMI# <<< H_SMI# <<<

17 H_A20M# <<< H_FERR# <<< H_IGNNE# <<< H_STPCLK# <<< H_INTR# <<< H_NMI# <<< H_SMI# <<<

TPAD30 TP49 RSVD CPU 1 M4 TPAD30 TP48 RSVD CPU 2 N5 TPAD30 TP47 RSVD CPU 3 T2 TPAD30 TP46 RSVD CPU 4 V3 TPAD30 TP89 RSVD CPU 5 B2 TPAD30 TP82 RSVD CPU 6 C3 TPAD30 TP87 RSVD CPU 7 D2 TPAD30 TP90 RSVD CPU 8 D22 TPAD30 TP88 RSVD CPU 9 D3 TPAD30 TP72 RSVD CPU 10 F6 TPAD30 TP93 RSVD CPU 11 B1

XDP TMS R102 1 54D9R2F-L1-GP

XDP TDI R101 1 54D9R2F-L1-GP

XDP BPM#5 R97 1 54D9R2F-L1-GP

H_CPURST# R116 1 51R2F-2-GP

XDP TRCK R94 1 54D9R2F-L1-GP

XDP TRST# R96 1 54D9R2F-L1-GP

All place within 2" to CPU

U33A 1 OF 4

H_A#3 J4C A3#
H_A#4 L5C A4#
H_A#5 L4C A5#
H_A#6 K5C A6#
H_A#7 M3C A7#
H_A#8 N2C A8#
H_A#9 J1C A9#
H_A#10 N3C A10#
H_A#11 P5C A11#
H_A#12 L2C A12#
H_A#13 L2C A13#
H_A#14 P4C A14#
H_A#15 P1C A15#
H_A#16 R1C A16#
M1C
H_REQ#0 K3C REQ#0#
H_REQ#1 H2C REQ#1#
H_REQ#2 K2C REQ#2#
H_REQ#3 J3C REQ#3#
H_REQ#4 L1C REQ#4#

H_A#17 Y2C A17#
H_A#18 U5C A18#
H_A#19 R3C A19#
H_A#20 W6C A20#
H_A#21 U4C A21#
H_A#22 Y5C A22#
H_A#23 U1C A23#
H_A#24 R4C A24#
H_A#25 T3C A25#
H_A#26 T3C A26#
H_A#27 W2C A27#
H_A#28 W5C A28#
H_A#29 Y4C A29#
H_A#30 U2C A30#
H_A#31 V4C A31#
H_A#32 W3C A32#
H_A#33 AA4C A33#
H_A#34 AB2C A34#
H_A#35 AA3C A35#
V1C
ADSTB#0#
REQ#0#
REQ#1#
REQ#2#
REQ#3#
REQ#4#
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H_HIT# R3C A19#
H_HIT# W6C A20#
H_HIT# U4C A21#
H_HIT# Y5C A22#
H_HIT# U1C A23#
H_HIT# R4C A24#
H_HIT# T3C A25#
H_HIT# T3C A26#
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H_HIT# U2C A30#
H_HIT# V4C A31#
H_HIT# W3C A32#
H_HIT# AA4C A33#
H_HIT# AB2C A34#
H_HIT# AA3C A35#
V1C
ADSTB#1#
A20M#
FERR#
IGNNE#
STPCLK#
LINT0
LINT1
SMI#

BGA479-SKT6-GPU4
62.10079.001

2nd: 62.10053.401

1005V_S0

54D9R2F-L1-GP

51R2F-2-GP

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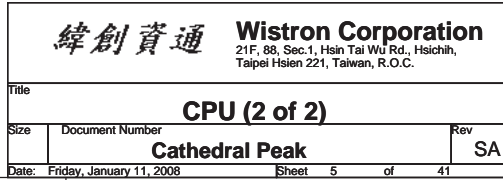
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54D9R2F-L1-GP

54D9R2F-L1-GP

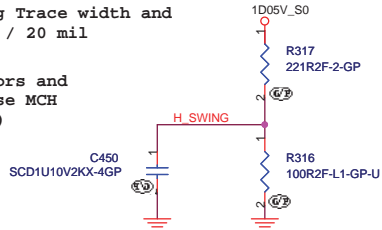
54D9R2F-L1-GP

54D9R2F-L1-GP



H_SWING routing Trace width and Spacing use 10 / 20 mil

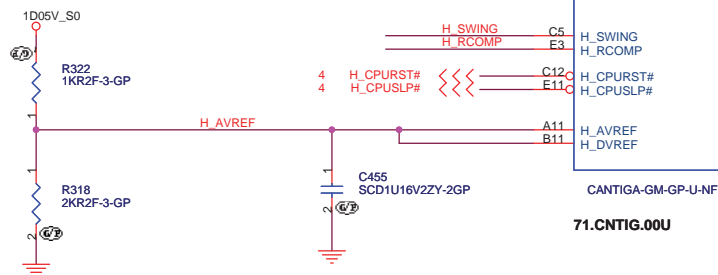
H_SWING Resistors and Capacitors close MCH
500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil

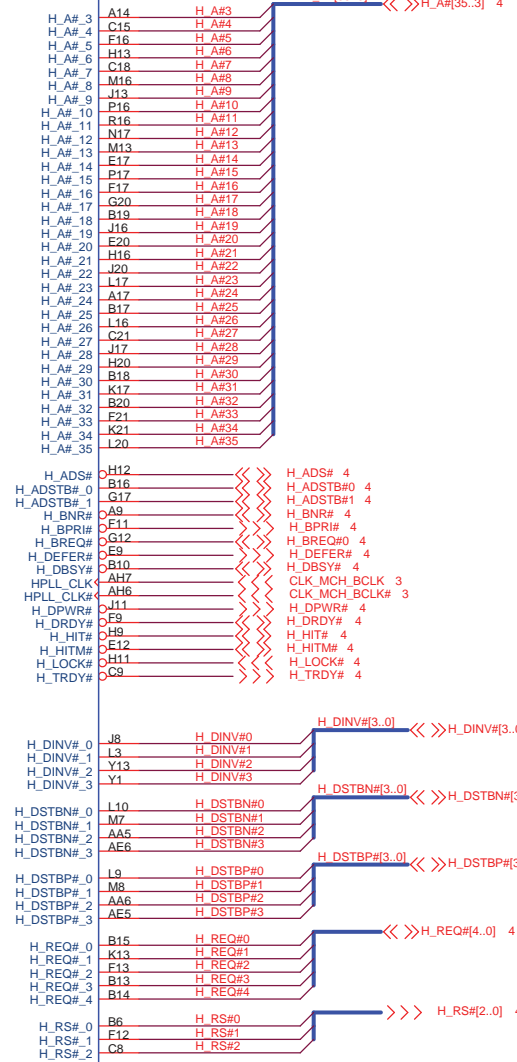


Place them near to the chip (< 0.5")

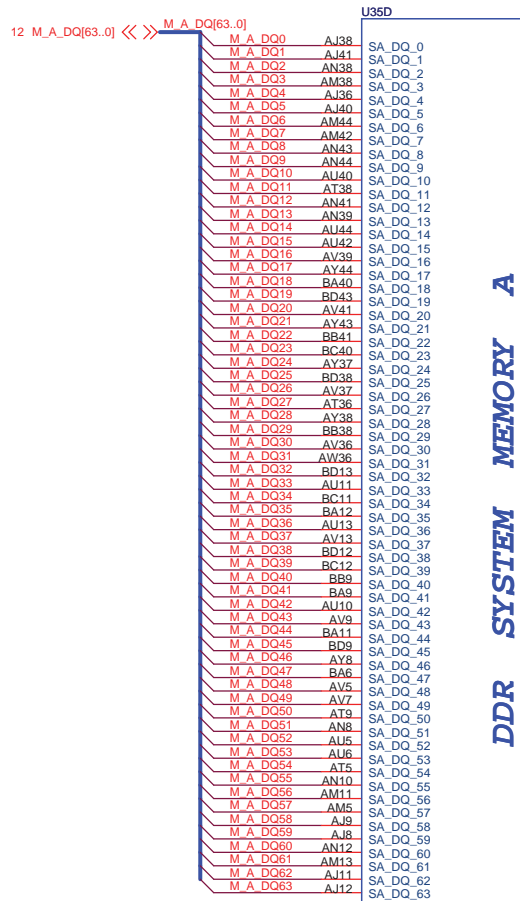


U35A 1 OF 10

HOST

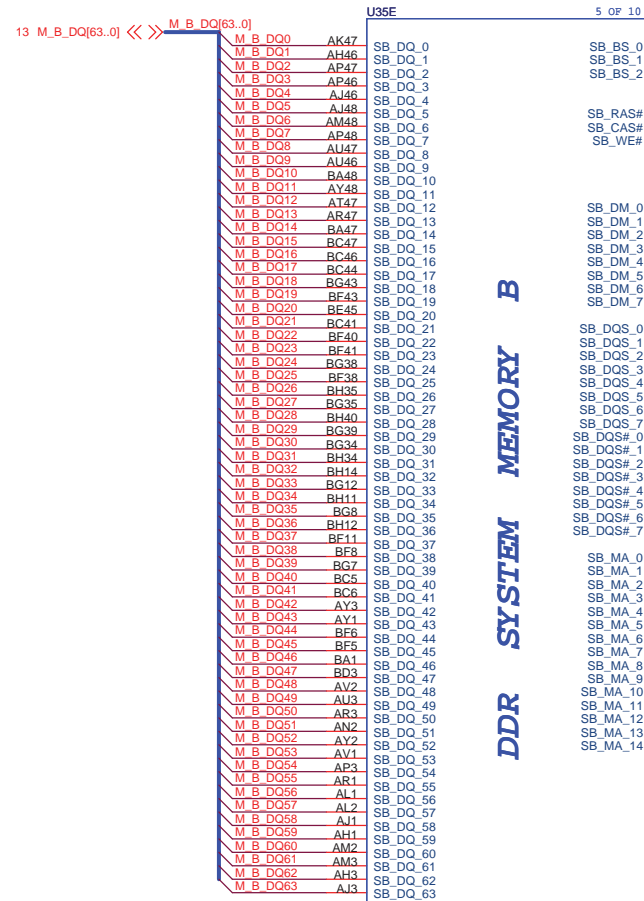


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CANTIGA-GM-GP-U-NF

71.CNTIG.00U



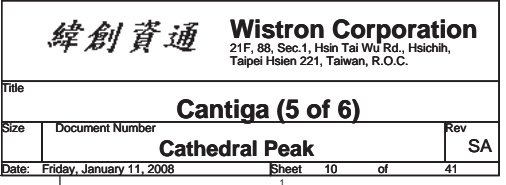
CANTIGA-GM-GP-U-NF

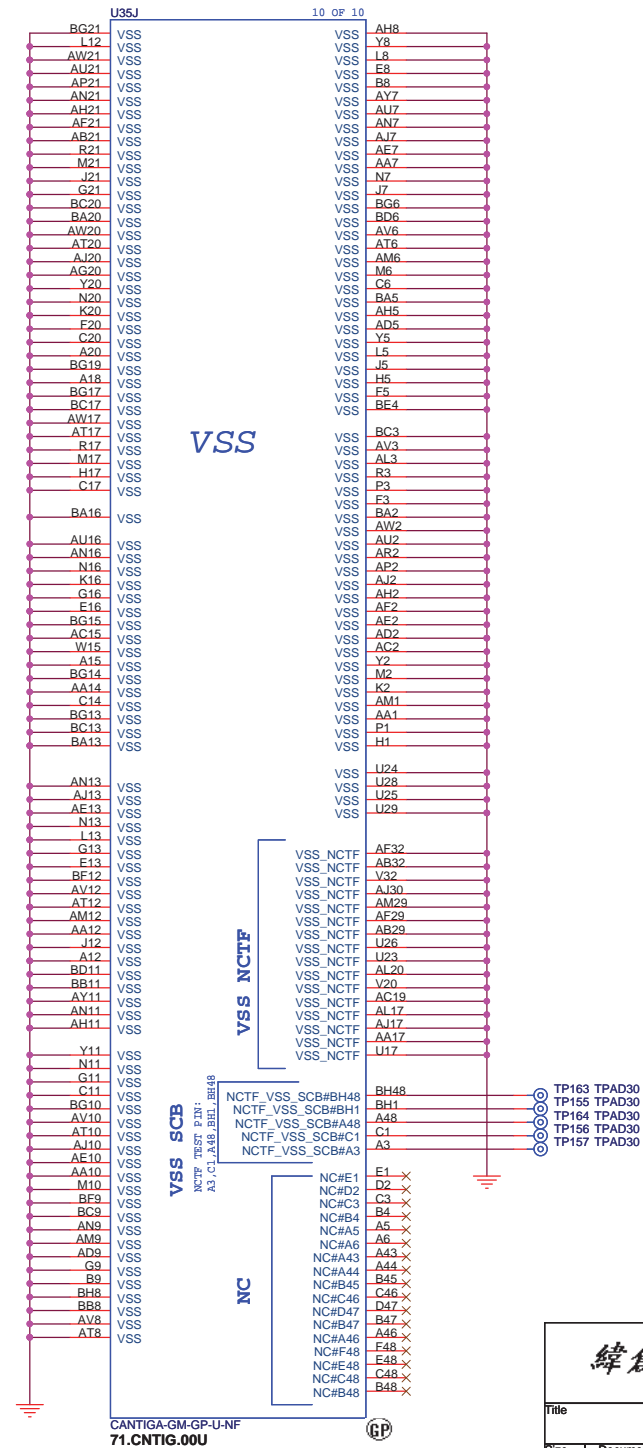
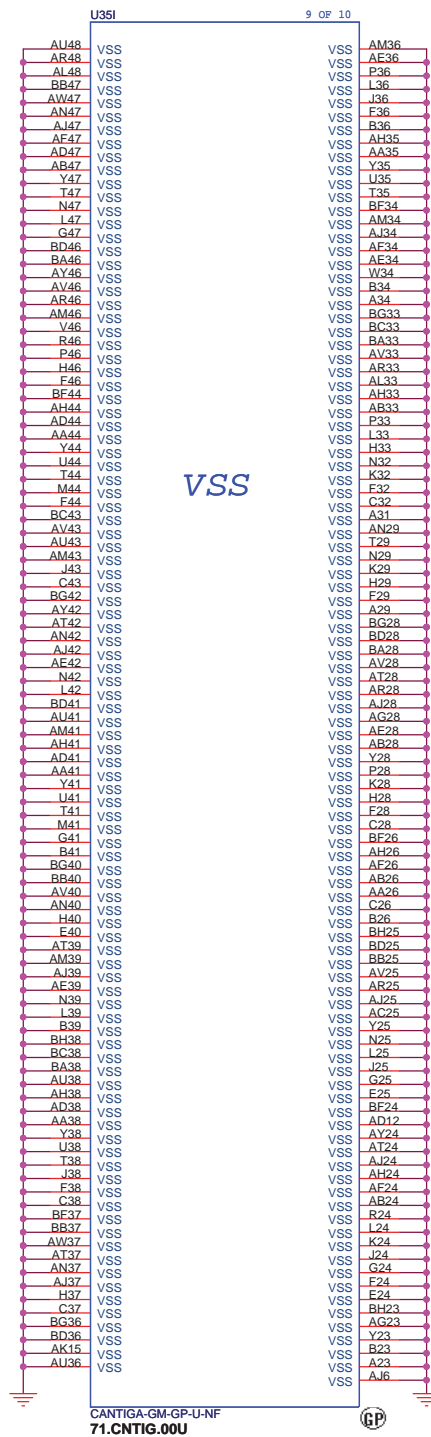
71.CNTIG.00U



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Taipei Hsien 221, Taiwan, R.O.C.

Title			SA
Cantiga (3 of 6)			
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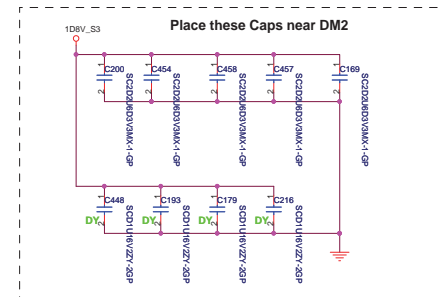


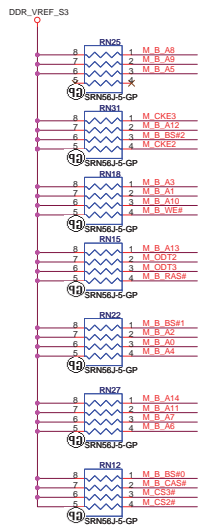
Put decap near power(0.9V) and pull-up resistor



Put decap near power(0.9V) and pull-up resistor

The diagram shows a horizontal power plane for 0.9V. It features a series of decoupling capacitors (C191, C188, C207, C181, C209, C218, C223, C182, C201, C173, C170) connected to a common ground rail on the right. A pull-up resistor is connected to the left end of the power plane. The components are labeled with their values and designators.



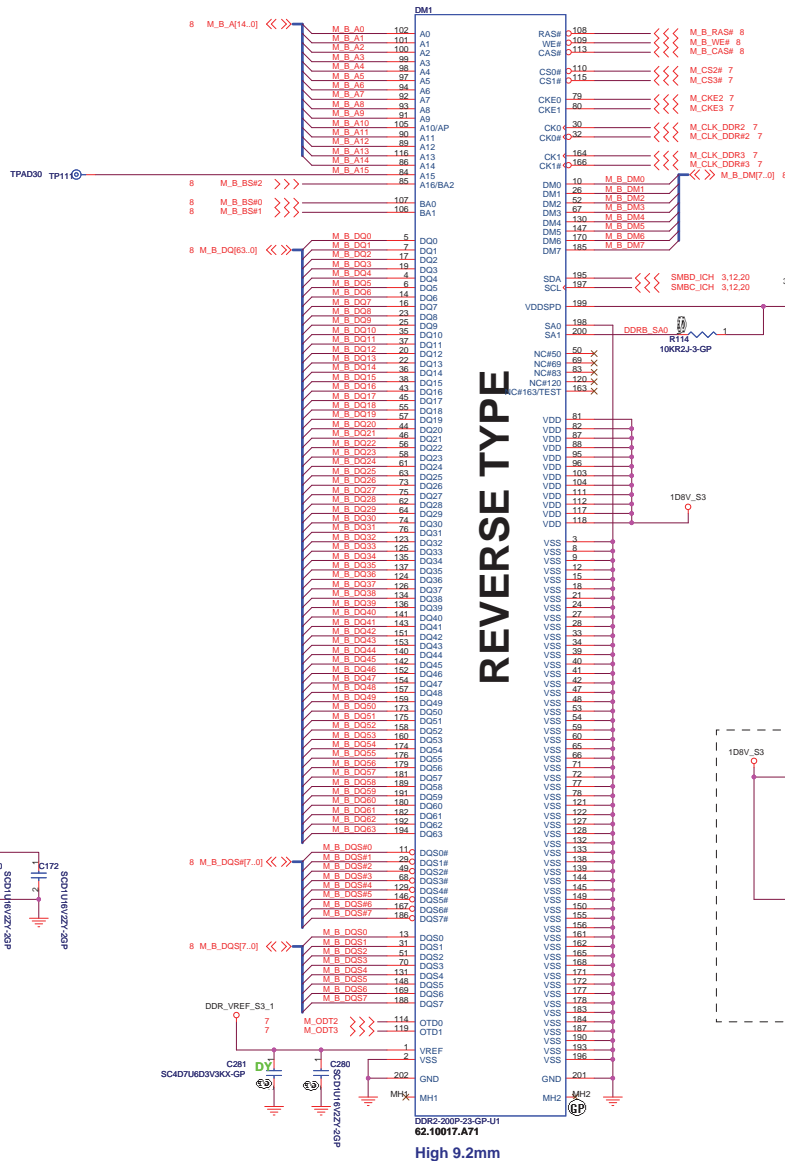
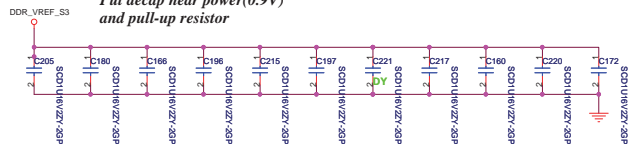


PARALLEL TERMINATION

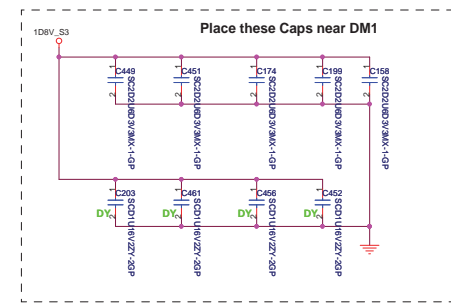
Put decap near power(0.9V) and pull-up resistor

Decoupling Capacitor

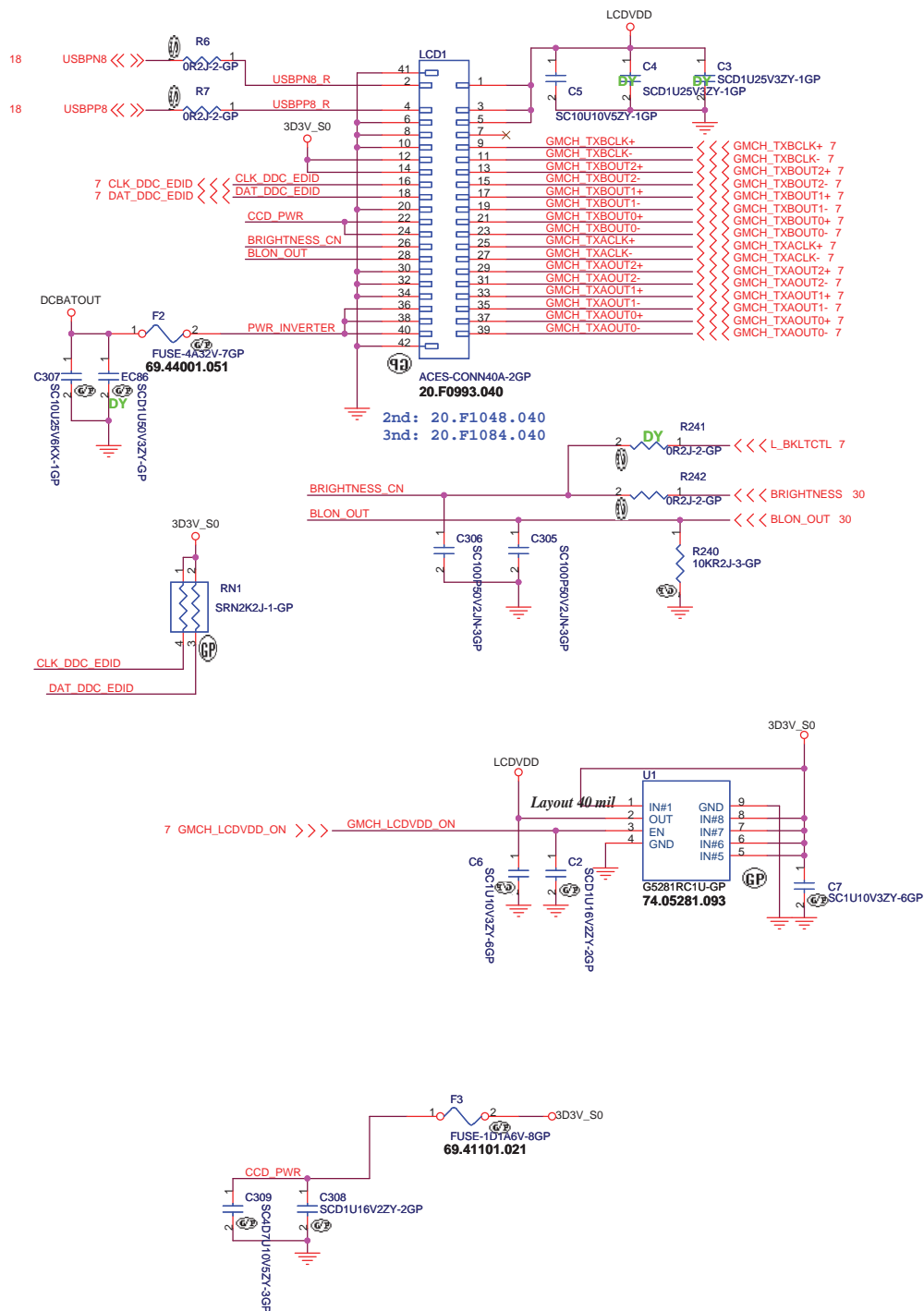
Put decap near power(0.9V) and pull-up resistor



REVERSE TYPE



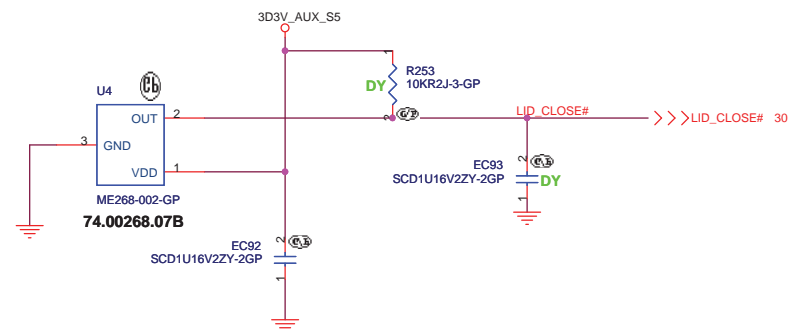
LCD/INVERTER/CCD CONN



Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND

Cover Up Switch



74.00268.A7B

74.00268.C7B

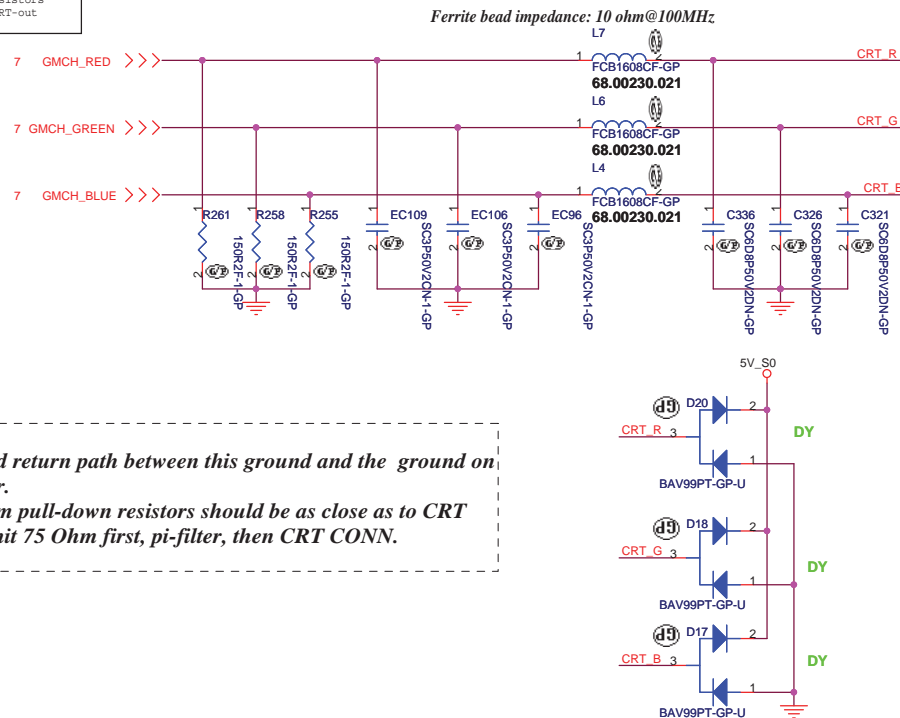
緯創資通

Wistron Corporation

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Title			
LCD CONN			
Size	Document Number	Rev	
		SA	
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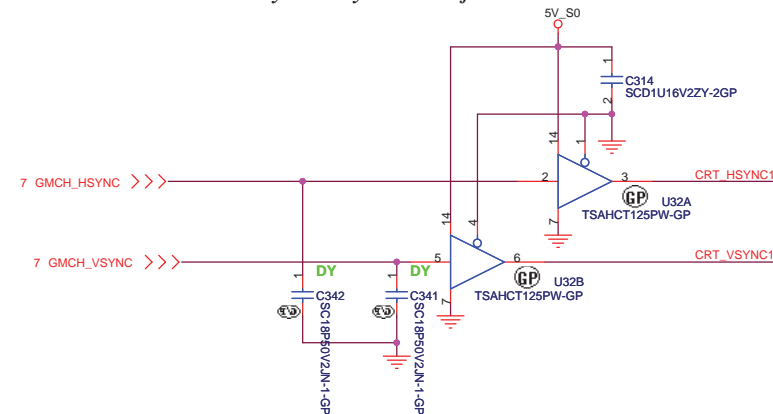
Layout Note:
Place these resistors
close to the CRT-out
connector



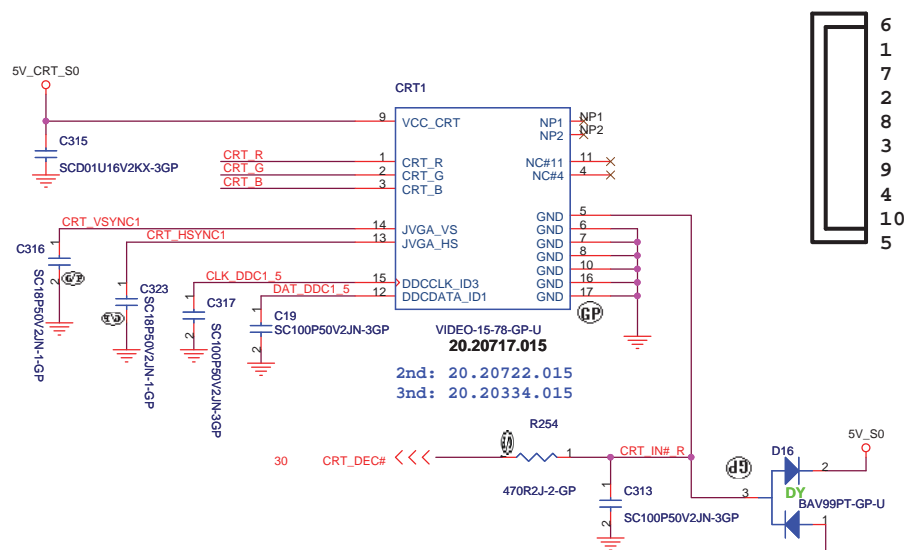
Layout Note:

* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

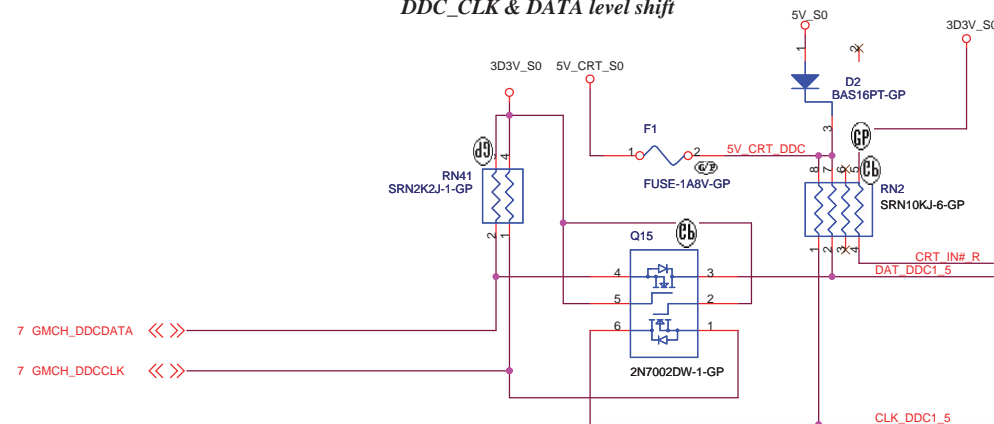
Hsync & Vsync level shift



CRT I/F & CONNECTOR

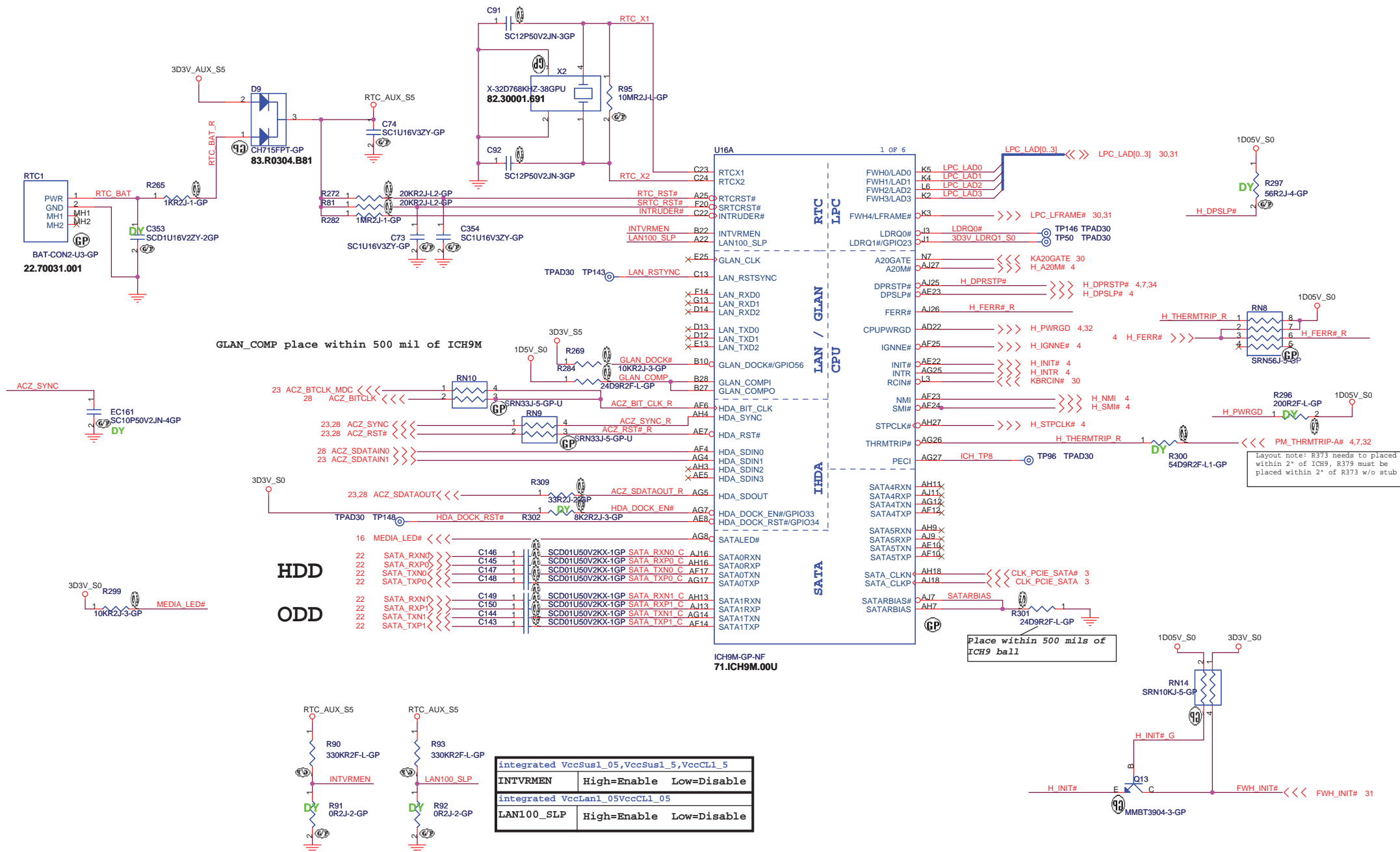


DDC_CLK & DATA level shift



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Title		
CRT Connector		
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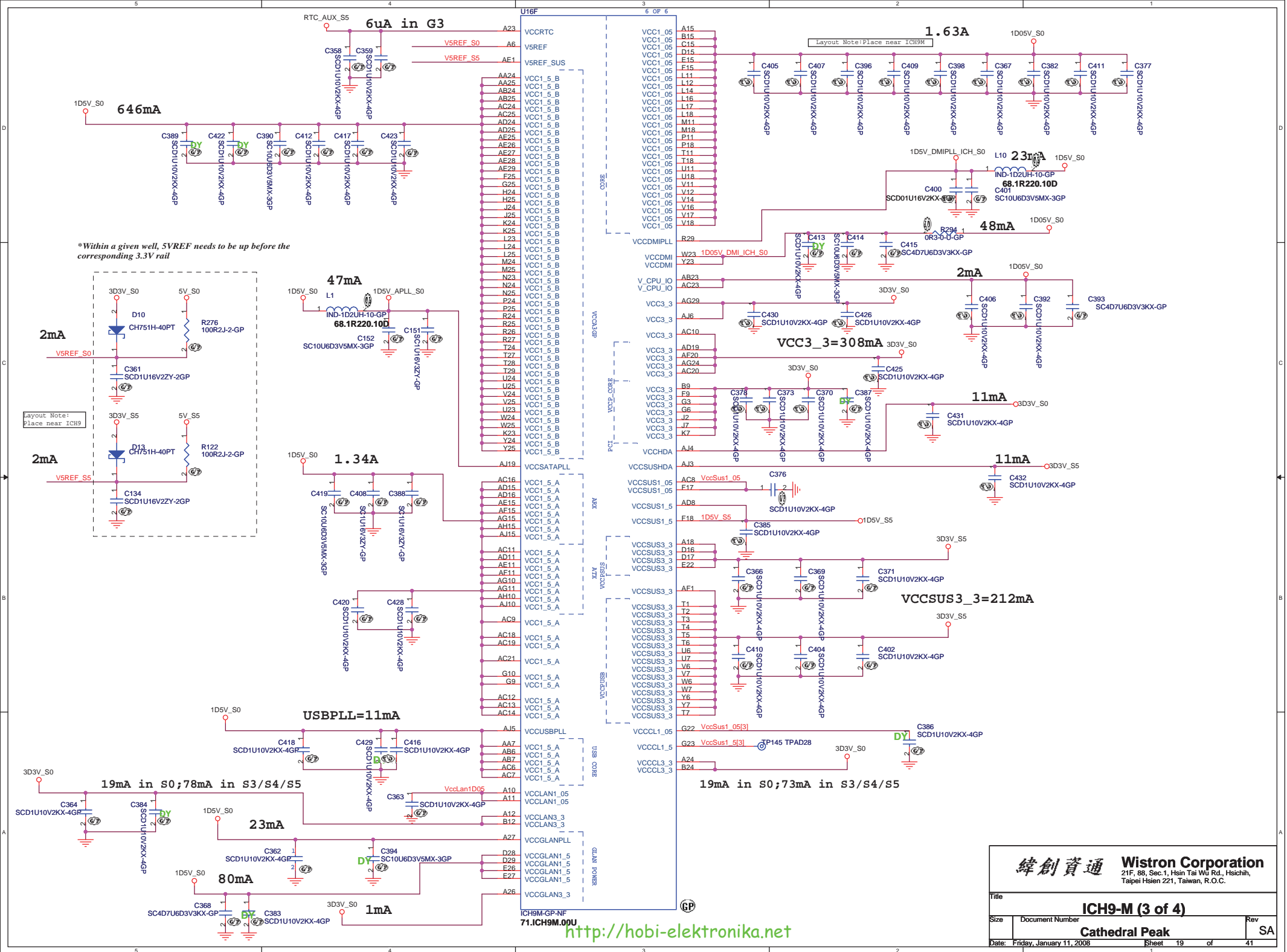
ICH9-M (1 of 4)

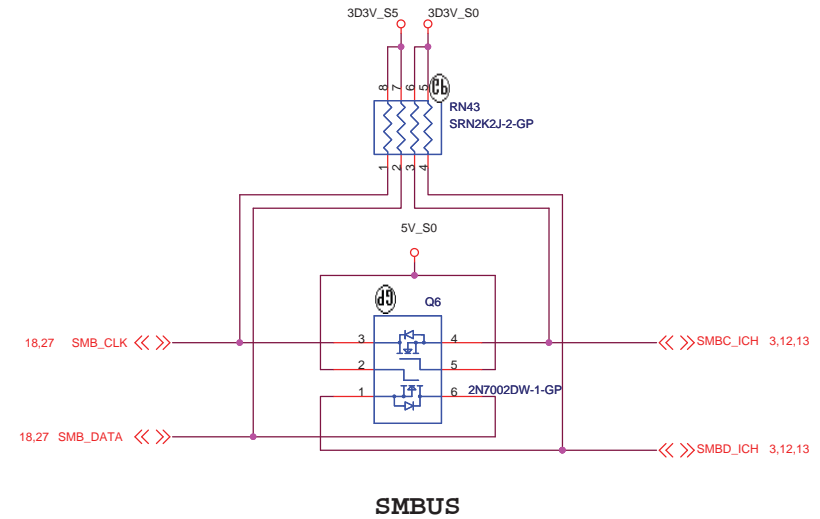
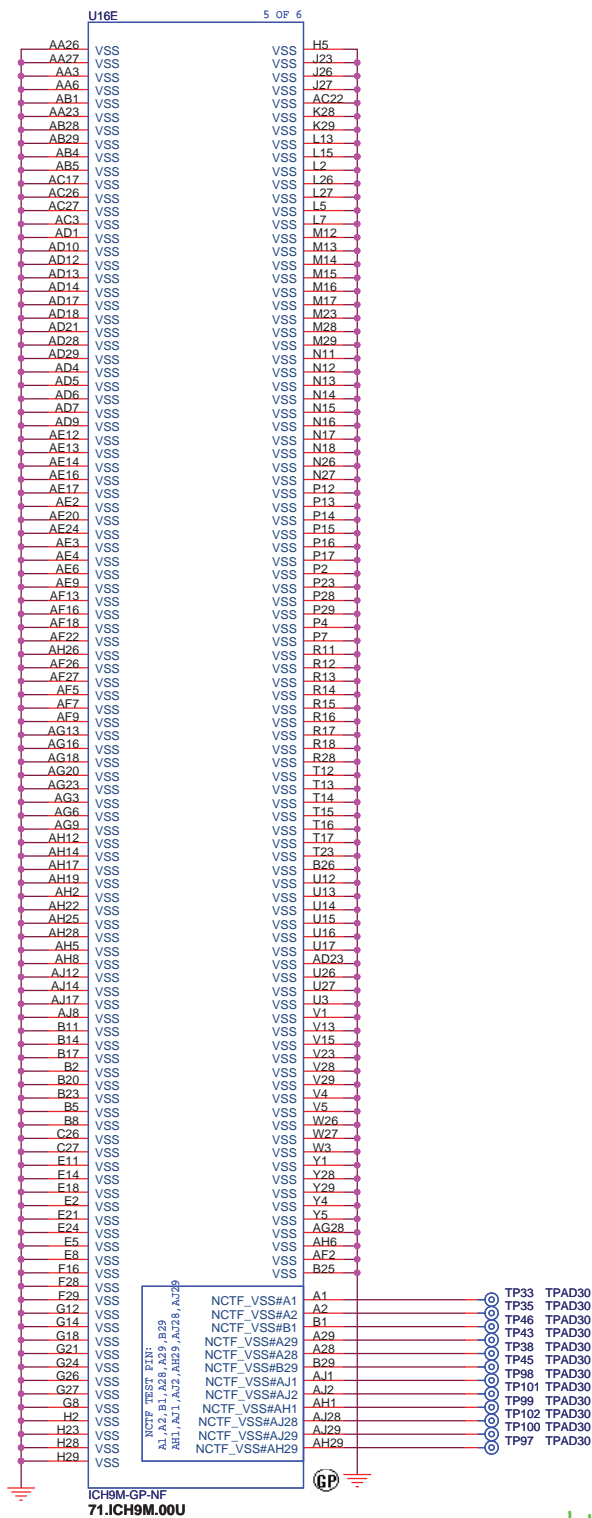
Size Document Number Rev SA

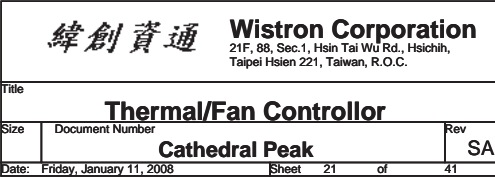
Cathedral Peak

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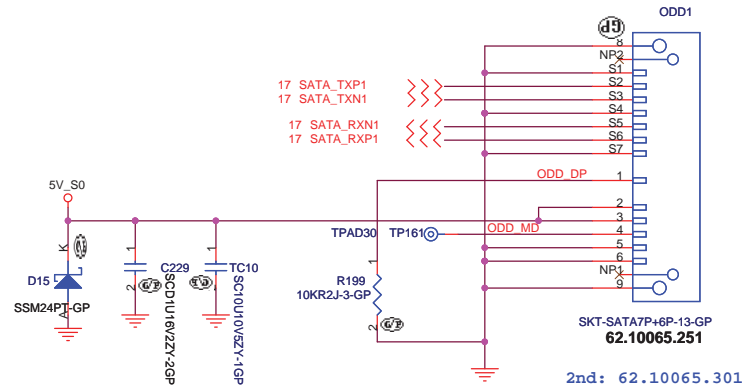




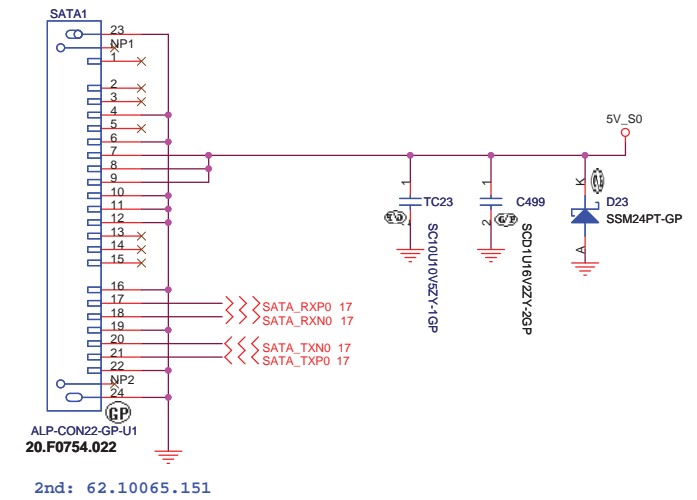




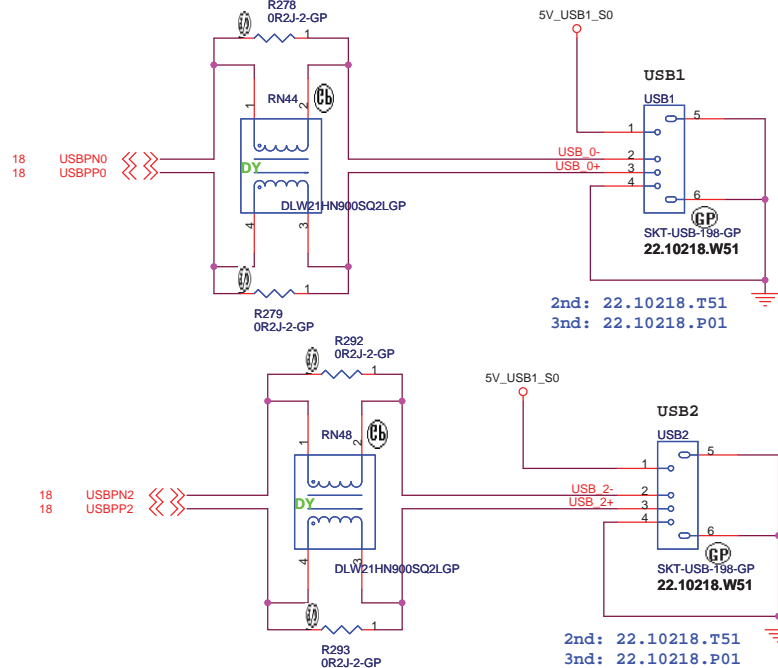
SATA ODD Connector



SATA Connector



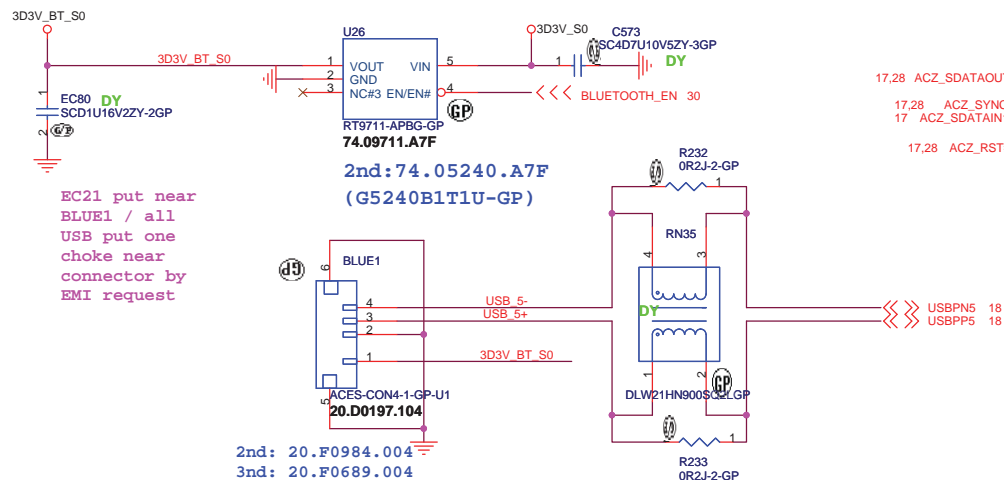
Co-Layout Common Mode Choke and 0 Ohm



Co-Layout Common Mode Choke and 0 Ohm

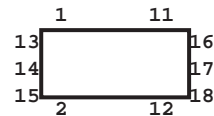
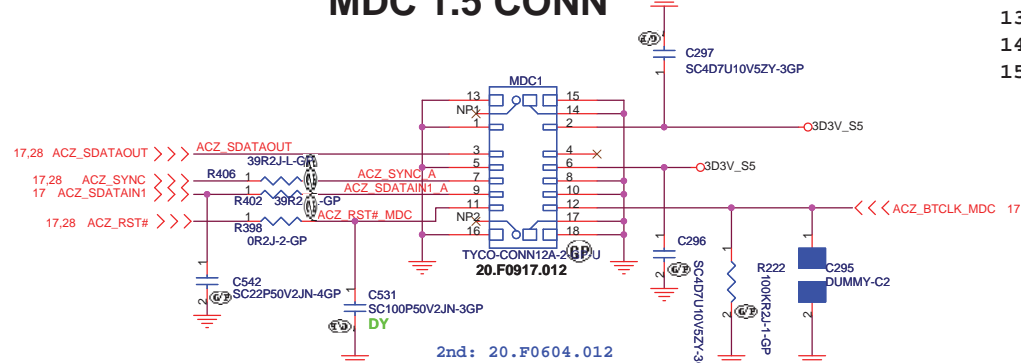
BLUETOOTH MODULE

1.5A / High Active Voltage 2V



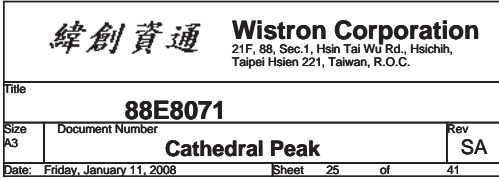
EC21 put near
BLUE1 / all
USB put one
choke near
connector by
EMI request

MDC 1.5 CONN



<http://hobi-elektronika.net>

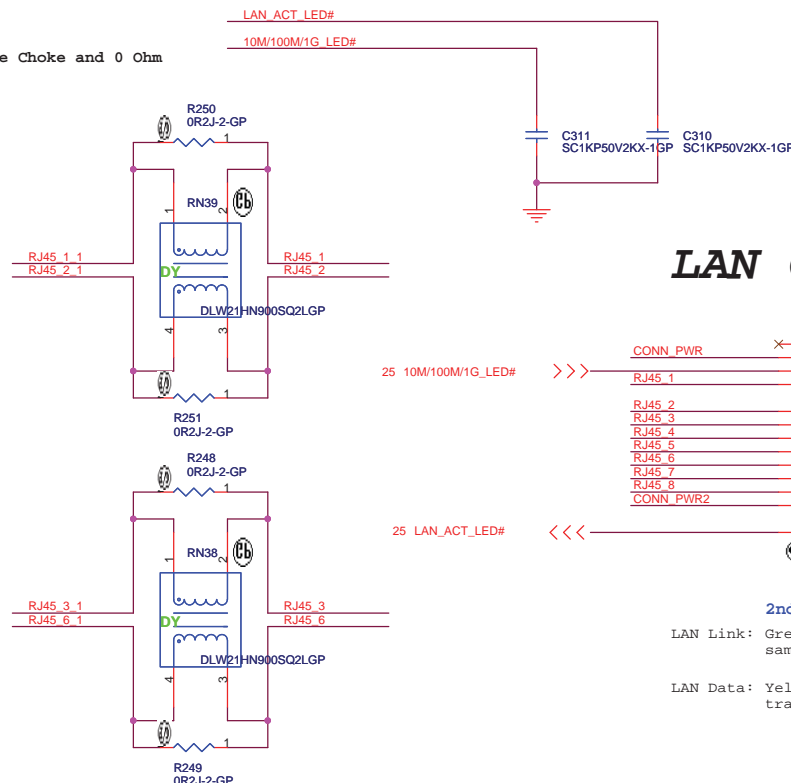
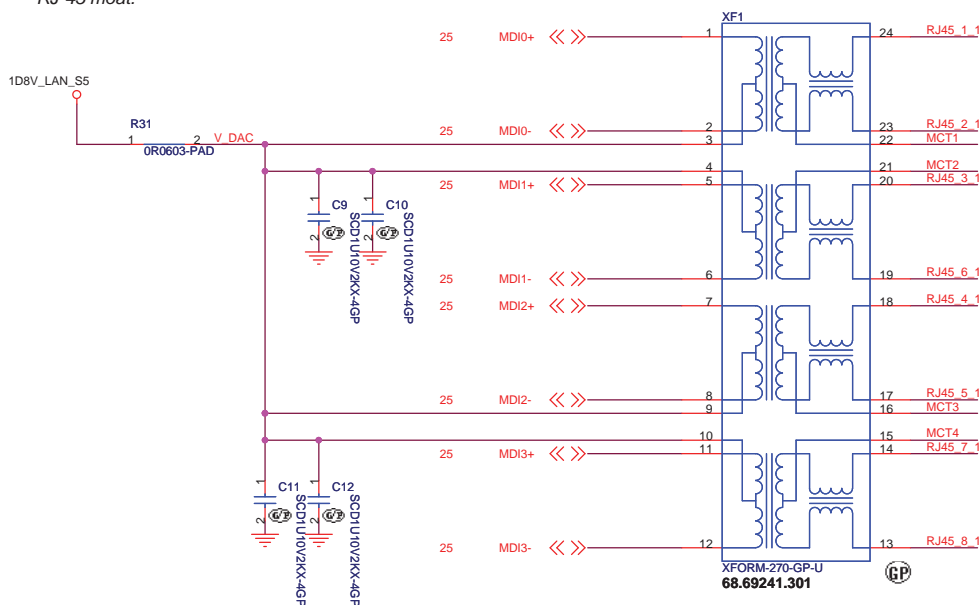
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
USB/BLUETOOTH/MDC	
Title Size Date: Friday, January 11, 2008	Document Number Cathedral Peak Sheet 23 of 41
Rev SA	74.09711.A7F



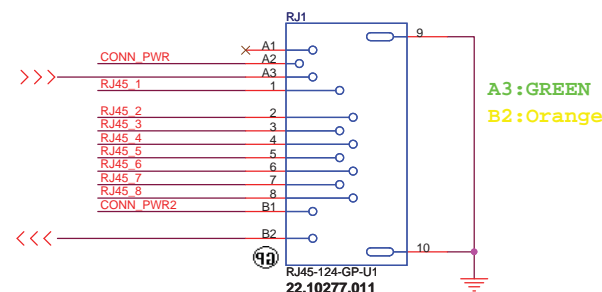
LAN Connector

- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat, except RJ-45 moat.

Co-Layout Common Mode Choke and 0 Ohm

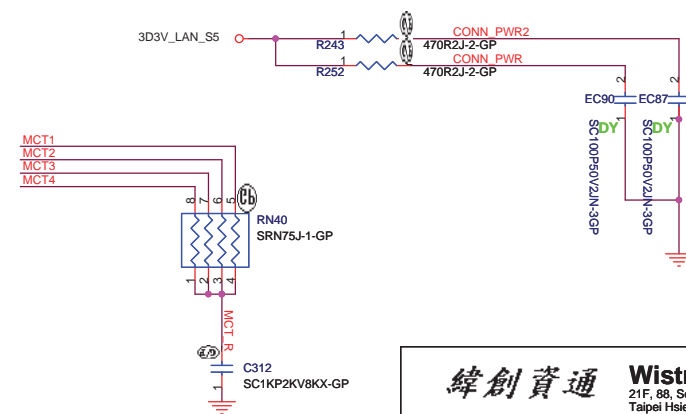
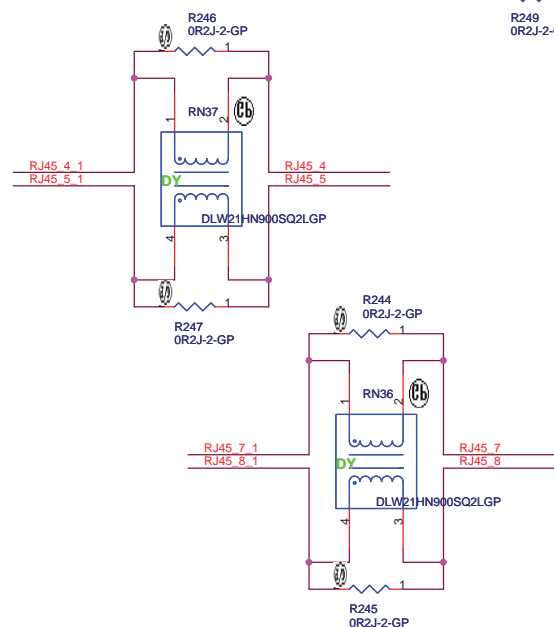


LAN Connector



2nd: 22.10277.061
LAN Link: Green(A3), behavior is the same for 10/100/1000 bits
LAN Data: Yellow(B2), when LAN is transferring data.

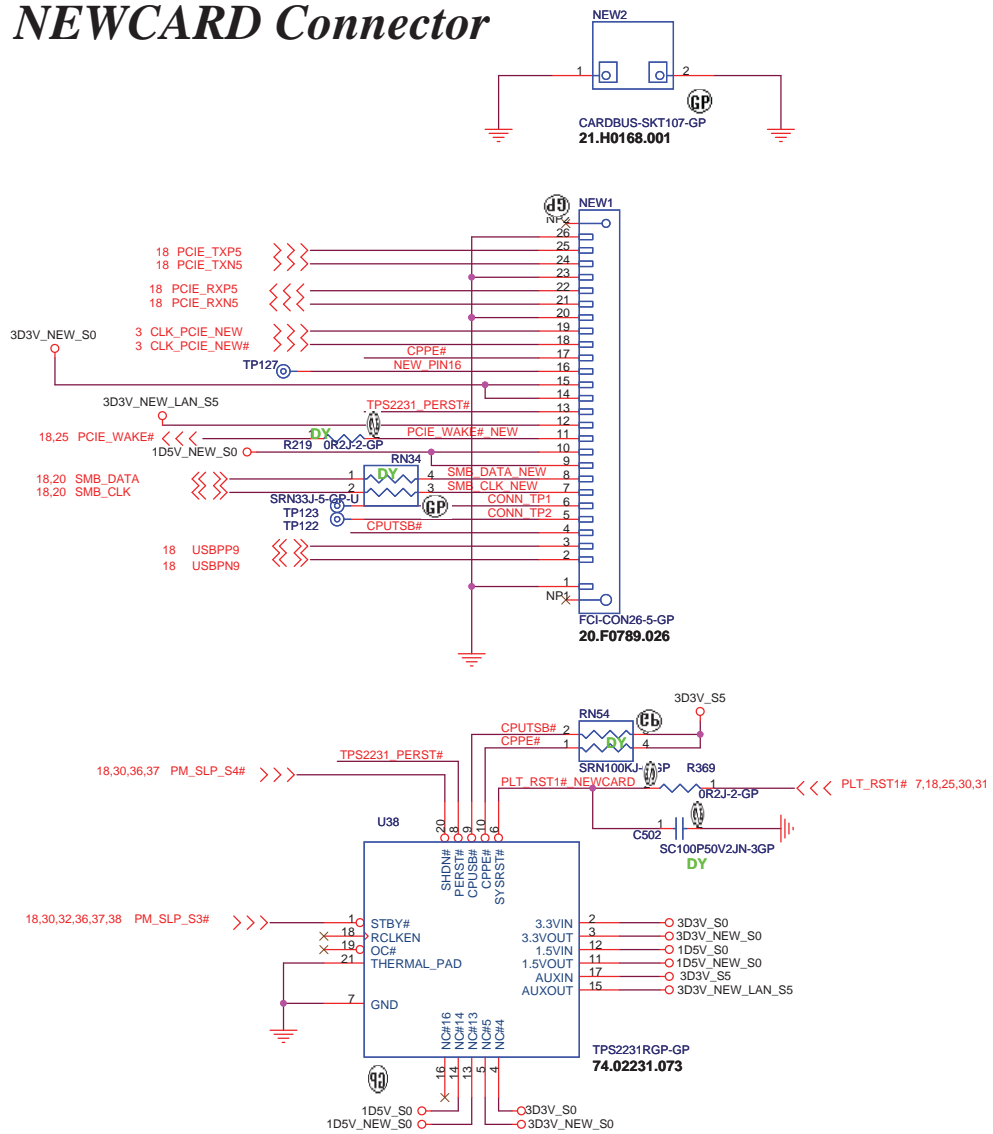
DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers



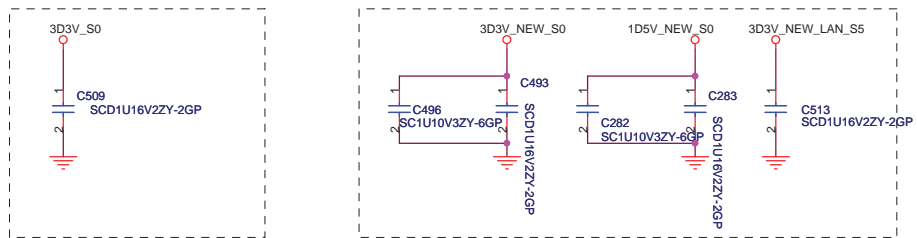
<http://hobi-elektronika.net>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
LAN CONN		
Size A3	Document Number	Rev SA
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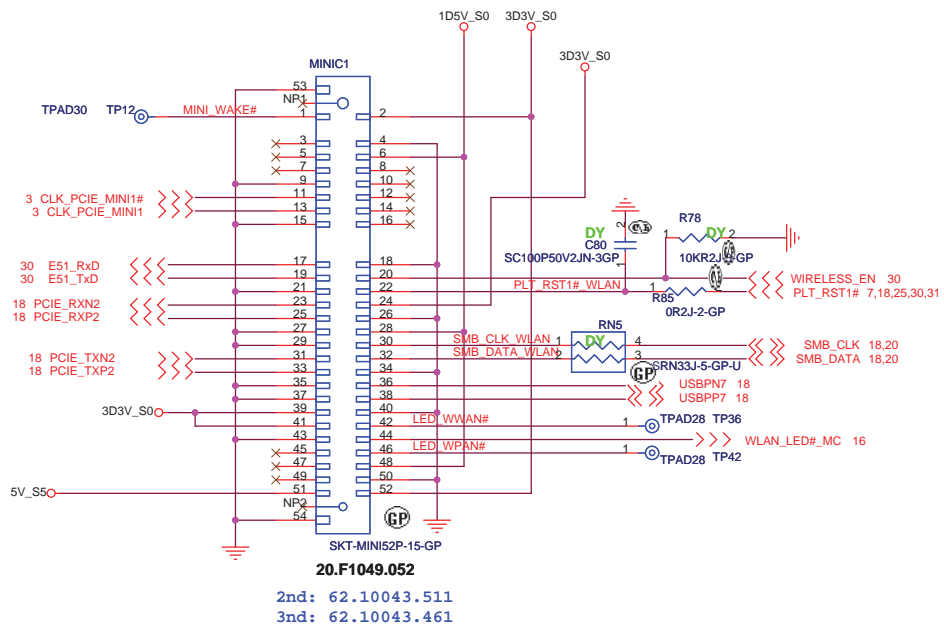
NEWCARD Connector



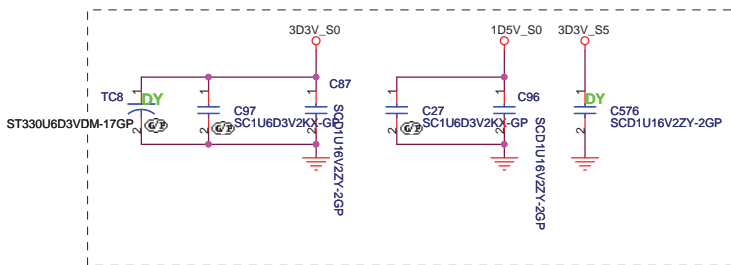
Place them Near to Connector



Mini Card Connector(WLAN)

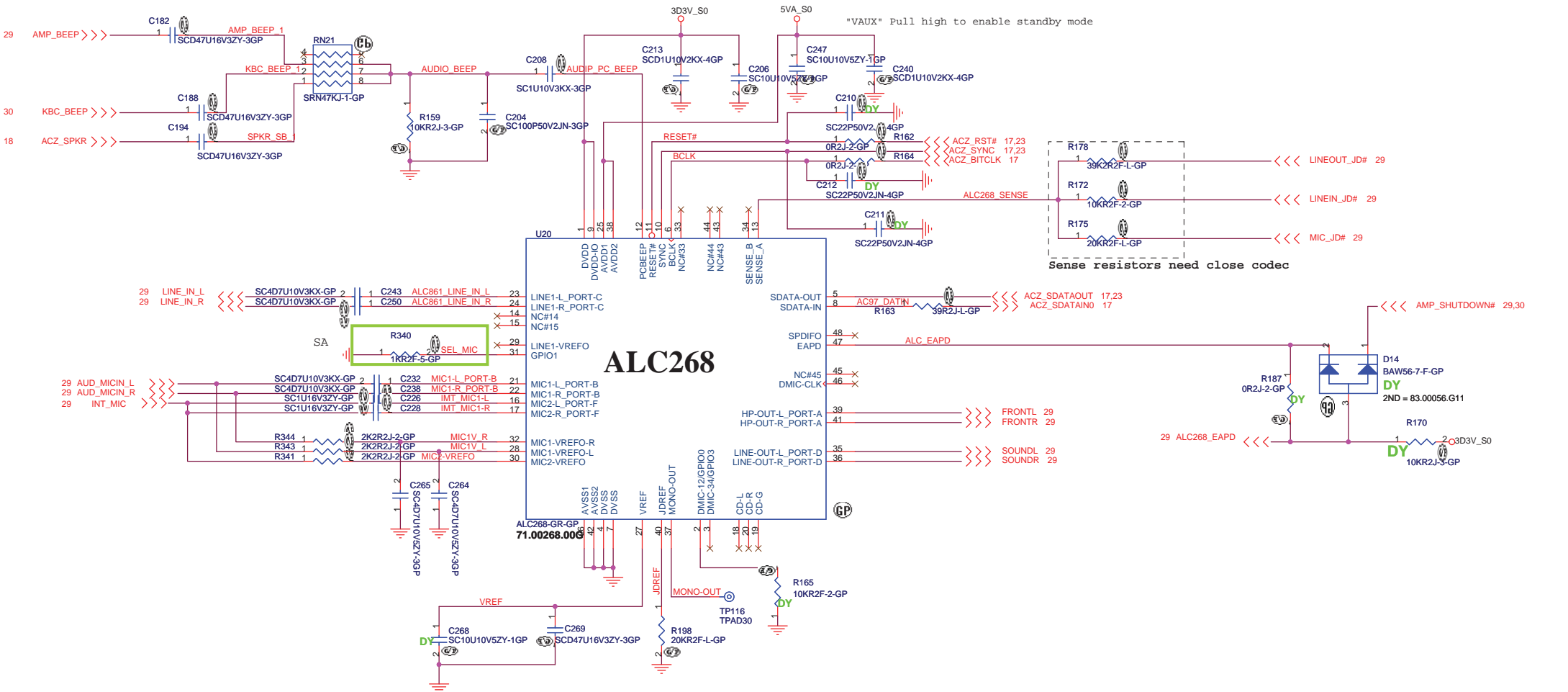


Place near MINIC1

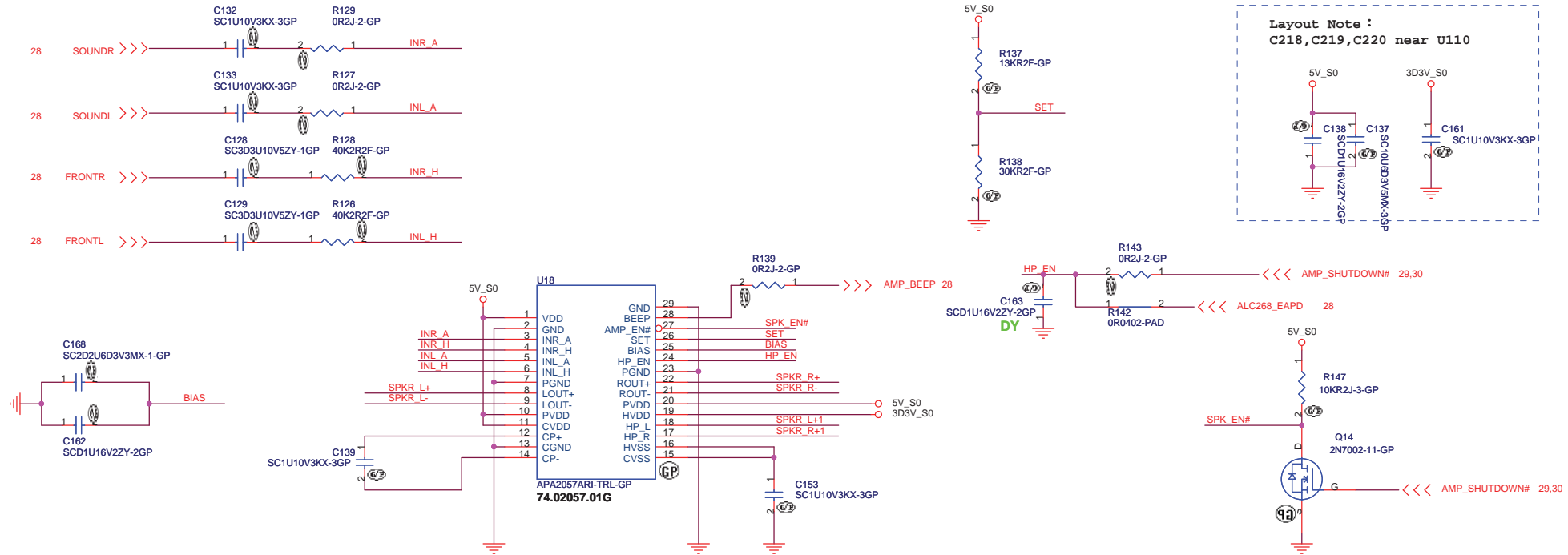


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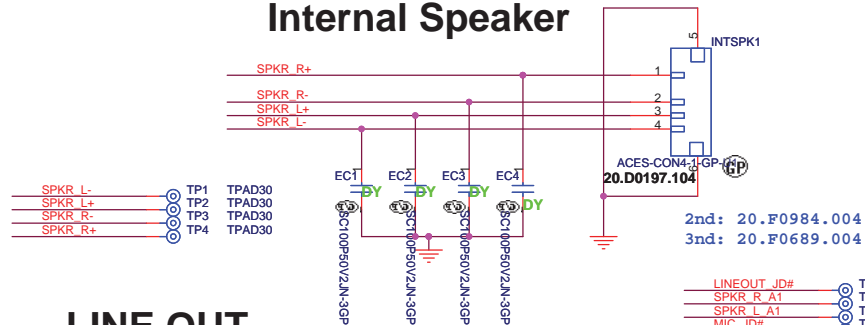
Title			
NEW CARD/MINI CARD			
Size	Document Number		Rev
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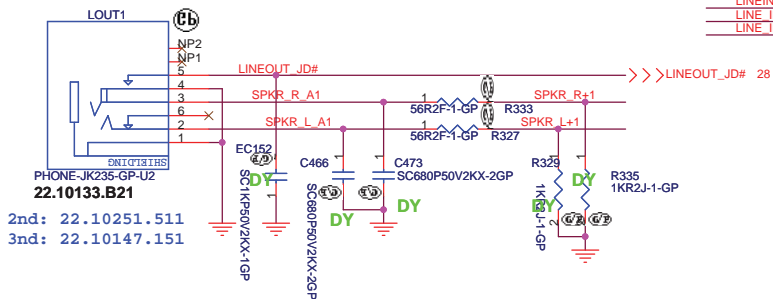
AUDIO OP AMPLIFIER



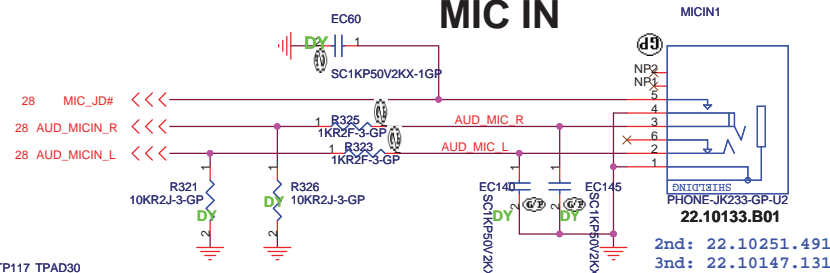
Internal Speaker



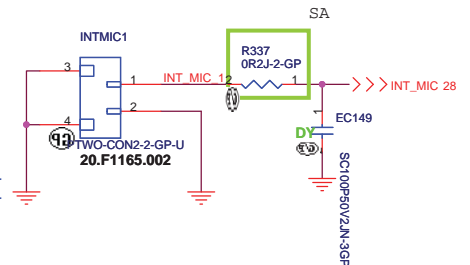
LINE OUT



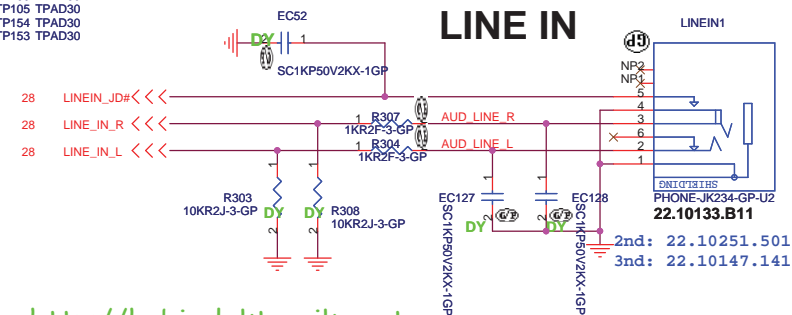
MIC IN



Analog Int. Mic

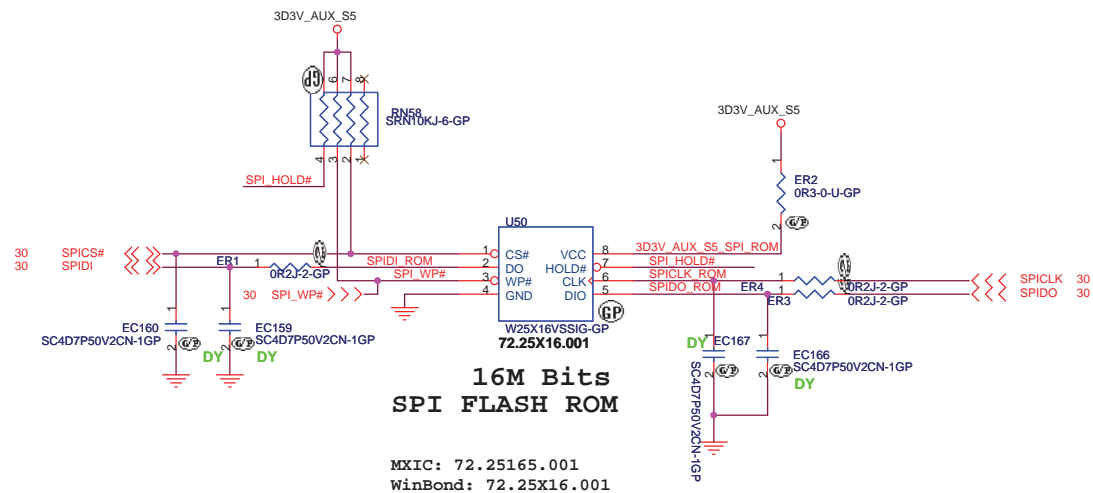


LINE IN

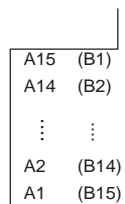


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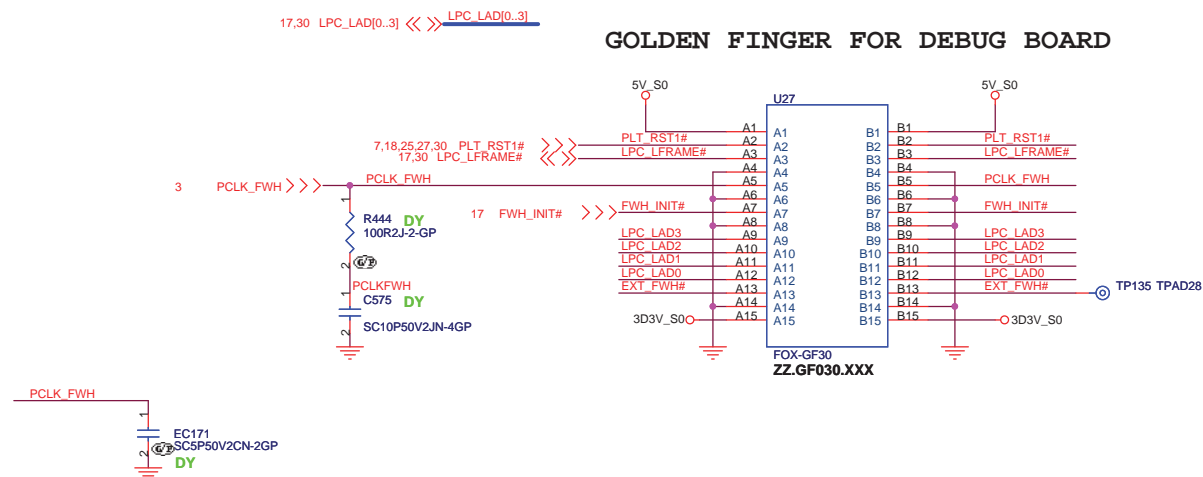
AUDIO AMP AND JACK			Rev
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TOP VIEW



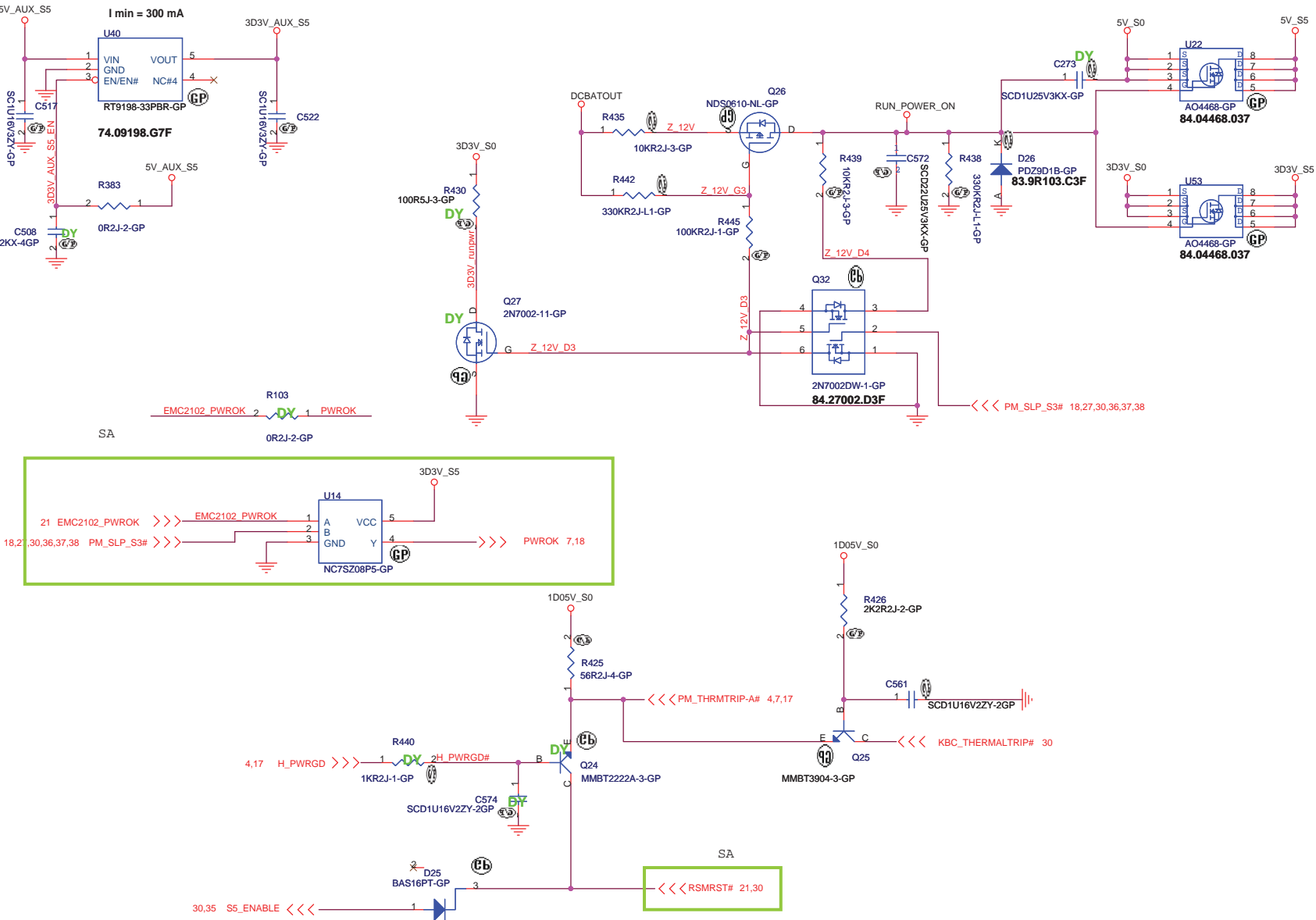
(BOTTOM VIEW)

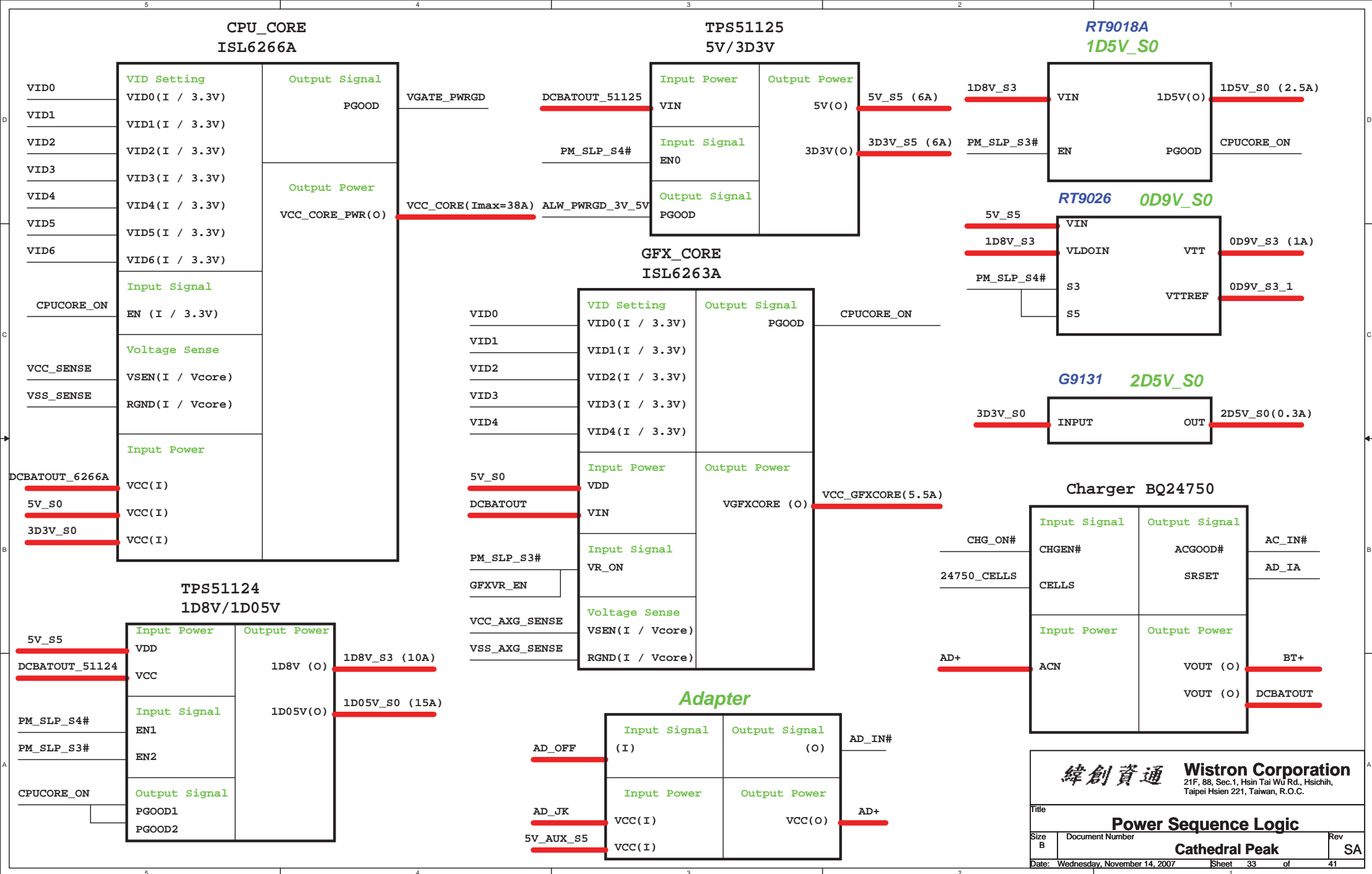


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Title			BIOS/GOLDEN FINGER	
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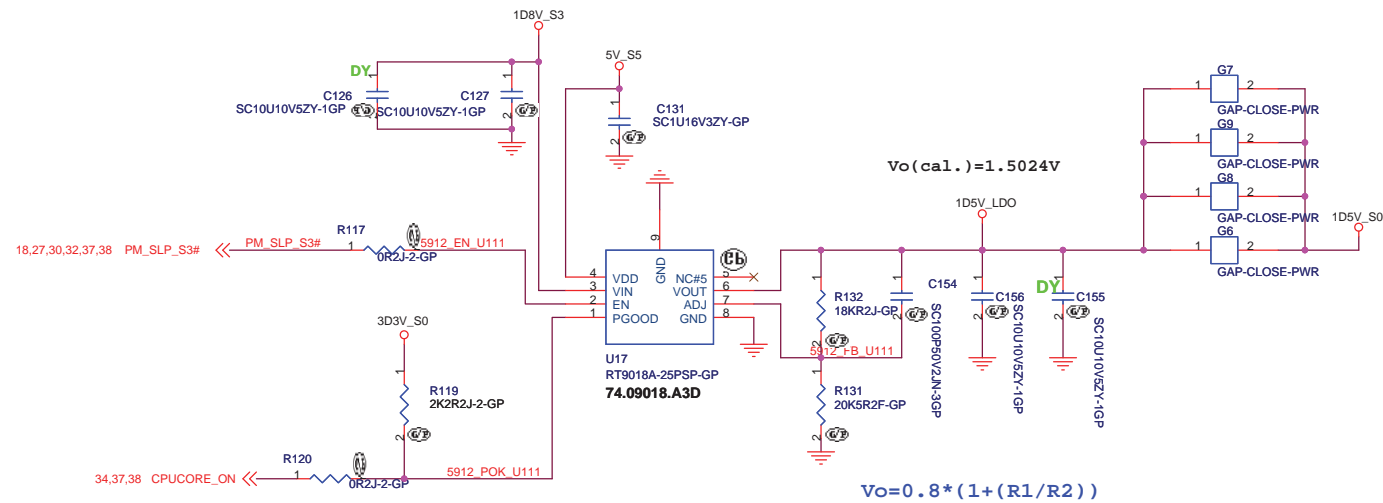
Run Power



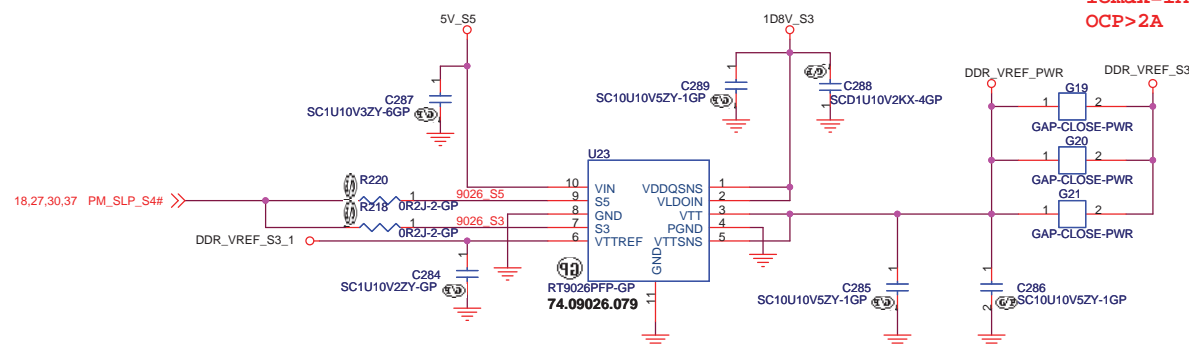


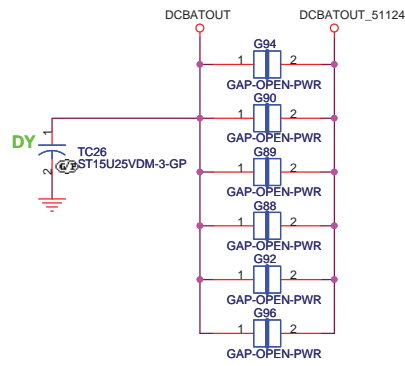


1D5V_S0
I_{omax}=2.5A

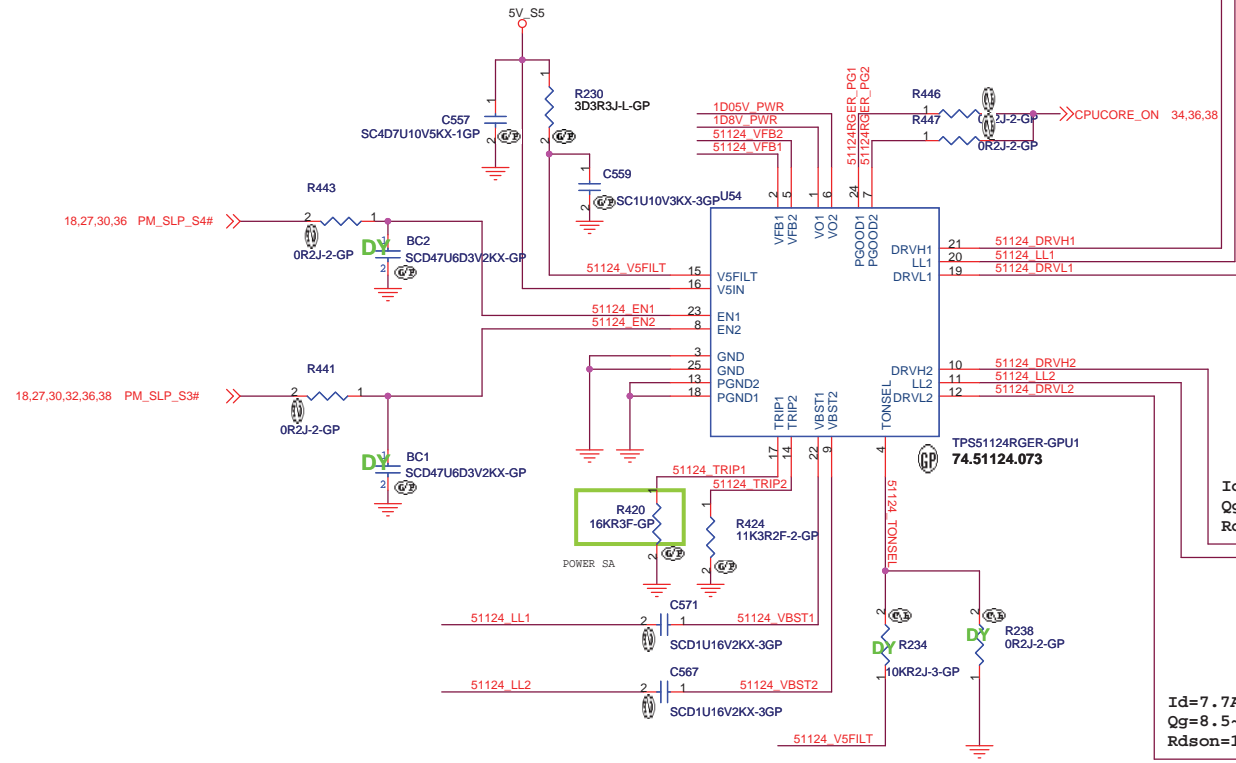


I_{omax}=1A
OCP>2A





$V_{trip}(mV) = R_{trip}(Kohm) * 10(uA)$
 $I_{ocp} = (V_{trip}/R_{dson}) + ((1/(2*L*f)) * ((V_{in}-V_{out}) * V_{out}) / V_{in}))$
 I/P cap: 10U 25V K1206 X5R/ 78.10622.52L



Id=7A
 Qg=8.7~13nC
 Rdson=23~30mohm

Id=7.7A
 Qg=8.5~13nC
 Rdson=16.5~21mohm

Id=7A
 Qg=8.7~13nC
 Rdson=23~30mohm

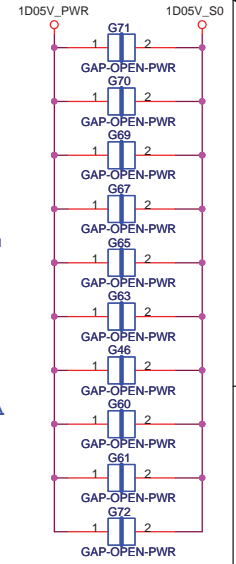
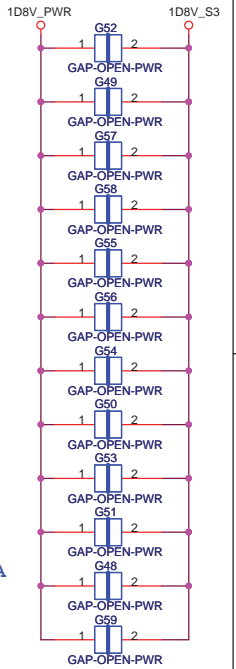
Id=7.7A
 Qg=8.5~13nC
 Rdson=16.5~21mohm

Cyntec 10*10*4
 DCR=4.2mohm, Irating=16A
 Isat=33A

1D8V Iomax=10A
 OCP>15A

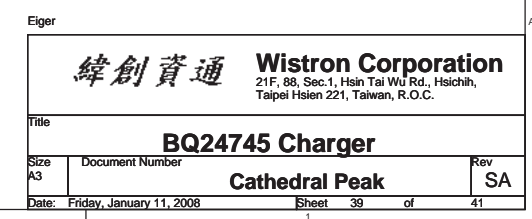
Cyntec 10*10*4
 DCR=4.2mohm, Irating=16A
 Isat=33A

1D05V Iomax=10.5A
 OCP>20A

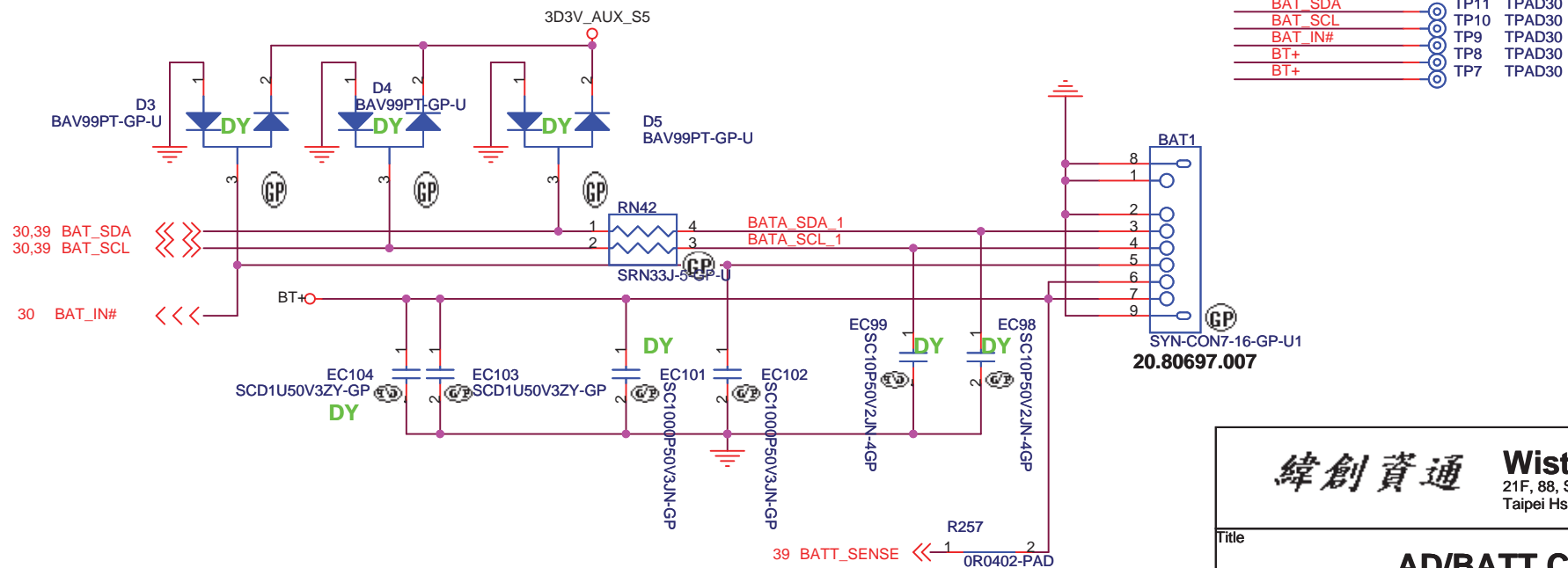


	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

Vout=0.758V*(R1+R2)/R2 --> PWM mode
 Vout=0.764V*(R1+R2)/R2 --> Skip Mode



BATTERY CONNECTOR



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Taipei Hsien 221, Taiwan, R.O.C.

AD/BATT CONN

Cathedral Peak

SA

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